

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 12 bit 250 MSPS analog to digital converter microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

<u>V62/10609</u> Drawing number	-	<u>01</u> Device type (See 1.2.1)	<u>X</u> Case outline (See 1.2.2)	<u>E</u> Lead finish (See 1.2.3)
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1.2.1 Device type(s).

<u>Device type</u>	<u>Generic</u>	<u>Circuit function</u>
01	ISLA112P25MREP	12 bit, 250 MSPS analog to digital converter

1.2.2 Case outline(s). The case outline(s) are as specified herein.

<u>Outline letter</u>	<u>Number of pins</u>	<u>JEDEC PUB 95</u>	<u>Package style</u>
X	72	See figure 1	Quad flat leadless plastic package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacture:

<u>Finish designator</u>	<u>Material</u>
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 2

1.3 Absolute maximum ratings. 1/

1.8 V analog supply (AVDD) to analog ground (AVSS)	-0.4 V to 2.1 V
1.8 V output supply (OVDD) to output ground (OVSS)	-0.4 V to 2.1 V
AVSS to OVSS	-0.3 V to 0.3 V
Analog inputs to AVSS	-0.4 V to AVDD + 0.3 V
Clock inputs to AVSS	-0.4 V to AVDD + 0.3 V
Logic inputs to AVSS	-0.4 V to OVDD + 0.3 V
Logic inputs to OVSS	-0.4 V to OVDD + 0.3 V
Junction temperature range (T _J)	+150°C
Storage temperature range (T _{STG})	-65°C to +150°C
Thermal resistance, junction to ambient (θ _{JA})	24°C/W 2/

1.4 Recommended operating conditions. 3/

Operating free-air temperature range (T _A)	-55°C to +125°C
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- 1/ Stresses beyond those listed under “absolute maximum rating” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- 2/ θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features.
- 3/ Use of this product beyond the manufacturers design rules or stated parameters is done at the user’s risk. The manufacturer and/or distributor maintain no responsibility or liability for product used beyond the stated limits.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 3

2. APPLICABLE DOCUMENTS

JEDEC PUB 95 – Registered and Standard Outlines for Semiconductor Devices

IPC/JEDEC J STD-020 - Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at <http://www.jedec.org>)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

- A. Manufacturer's name, CAGE code, or logo
- B. Pin 1 identifier
- C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Logic diagram. The logic diagram shall be as shown in figure 3.

3.5.4 Timing waveforms. The timing waveforms shall be as shown in figures 4, 5, 6, 7, 8, 9, 10, and 11.

3.5.5 Application information. Detailed application information may be found in the manufacturer's datasheet.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 4

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits <u>3/</u>		Unit
					Min	Max	
DC specifications							
Analog input section							
Full scale analog input range	V _{FS}	Differential	-55°C to +125°C	01	1.36	1.59	V _{PP}
Input resistance	R _{IN}	Differential	+25°C	01	1000 typical		Ω
Input capacitance	C _{IN}	Differential	+25°C	01	1.9 typical		pF
Full scale range temperature drift	A _{VTC}		+125°C	01	90 typical		ppm / °C
Input offset voltage	V _{OS}		-55°C to +125°C	01	-10	10	mV
Gain error	EG		+25°C	01	2 typical		%
Common mode output voltage	V _{CM}		+25°C	01	0.435	0.635	V
Clock input section							
Inputs common mode voltage			+25°C	01	0.9 typical		V
CLKP, CLKN input swing			+25°C	01	1.8 typical		V
Power requirements section							
1.8 V analog supply voltage	AVDD		-55°C to +125°C	01	1.7	1.9	V
1.8 V digital supply voltage	OVDD		-55°C to +125°C	01	1.7	1.9	V
1.8 V analog supply current	I _{AVDD}		-55°C to +125°C	01		96	mA
1.8 V digital supply current (SDR) <u>4/</u>	I _{OVDD}	3 mA low voltage differential signaling (LVDS)	-55°C to +125°C	01		76	mA
1.8 V digital supply current (DDR) <u>4/</u>	I _{OVDD}	3 mA LVDS	+25°C	01	39 typical		mA
Power supply rejection ratio	PSRR	30 MHz, 200 V _{PP} signal on AVDD	+25°C	01	-36 typical		dB

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 5

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits <u>2/</u>		Unit
					Min	Max	
DC specifications - continued.							
Total power dissipation section							
Normal mode (SDR)	PD	3 mA LVDS	-55°C to +125°C	01		310	mW
Normal mode (DDR)	PD	3 mA LVDS	+25°C	01	234 typical		mW
Nap mode	PD		-55°C to +125°C	01		92	mW
Sleep mode	PD	CSB at logic high	-55°C to +125°C	01		18	mW
Nap mode <u>5/</u> wakeup time		Sample clock running	+25°C	01	1 typical		μs
Sleep mode <u>5/</u> wakeup time		Sample clock running	+25°C	01	1 typical		ms
AC specifications <u>6/</u>							
Differential nonlinearity	DNL		-55°C to +125°C	01	-0.9	+0.9	LSB
Integral nonlinearity	INL		-55°C to +125°C	01	-2.0	+2.0	LSB
Minimum <u>7/</u> conversion rate	f _S MIN		-55°C to +125°C	01		40	MSPS
Maximum conversion rate	f _S MAX		-55°C to +125°C	01	250		MSPS
Signal to noise ratio	SNR	f _{IN} = 10 MHz	+25°C	01	66.1 typical		dBFS
		f _{IN} = 105 MHz	-55°C to +125°C		62.7		
		f _{IN} = 190 MHz	+25°C		65.9 typical		
		f _{IN} = 364 MHz	+25°C		65.4 typical		
		f _{IN} = 695 MHz	+25°C		63.8 typical		
		f _{IN} = 995 MHz	+25°C		62.6 typical		

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 6

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits <u>3/</u>		Unit
					Min	Max	
AC specifications - continued. <u>6/</u>							
Signal to noise and distortion	SINAD	f _{IN} = 10 MHz	+25°C	01	65.3 typical		dBFS
		f _{IN} = 105 MHz	-55°C to +125°C		62.2		
		f _{IN} = 190 MHz	+25°C		64.6 typical		
		f _{IN} = 364 MHz	+25°C		63.9 typical		
		f _{IN} = 695 MHz	+25°C		56.9 typical		
		f _{IN} = 995 MHz	+25°C		49.6 typical		
Effective number of bits	ENOB	f _{IN} = 10 MHz	+25°C	01	10.6 typical		Bits
		f _{IN} = 105 MHz	-55°C to +125°C		10.1		
		f _{IN} = 190 MHz	+25°C		10.4 typical		
		f _{IN} = 364 MHz	+25°C		10.3 typical		
		f _{IN} = 695 MHz	+25°C		9.2 typical		
		f _{IN} = 995 MHz	+25°C		7.9 typical		
Spurious free dynamic range	SFDR	f _{IN} = 10 MHz	+25°C	01	83.0 typical		dBc
		f _{IN} = 105 MHz	-55°C to +125°C		67		
		f _{IN} = 190 MHz	+25°C		79 typical		
		f _{IN} = 364 MHz	+25°C		76 typical		
		f _{IN} = 695 MHz	+25°C		61 typical		
		f _{IN} = 995 MHz	+25°C		51 typical		

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 7

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits <u>3/</u>		Unit
					Min	Max	
AC specifications - continued. <u>6/</u>							
Intermodulation distortion	IMD	f _{IN} = 70 MHz	+25°C	01	-86 typical		dBFS
		f _{IN} = 170 MHz	+25°C		-97 typical		
Word error rate	WER		+25°C	01	10 ⁻¹² typical		
Full power dissipation	FPBW		+25°C	01	1300 typical		MHz
Digital specifications							
Inputs section							
Input current high (SDIO, RESETN)	I _{IH}	V _{IN} = 1.8 V	-55°C to +125°C	01	-1	1	μA
Input current low (SDIO, RESETN)	I _{IL}	V _{IN} = 0 V	-55°C to +125°C	01	-25	-5	μA
Input voltage high (SDIO, RESETN)	V _{IH}		-55°C to +125°C	01	1.17		V
Input voltage low (SDIO, RESETN)	V _{IL}		-55°C to +125°C	01		0.63	V
Input current high <u>8/</u> (OUTMODE, NAPSLP, CLKDIV, OUTFMT)	I _{IH}		-55°C to +125°C	01	15	40	μA
Input current low (OUTMODE, NAPSLP, CLKDIV, OUTFMT)	I _{IL}		-55°C to +125°C	01	-40	-15	μA
Input capacitance	C _{DI}		+25°C	01	3 typical		pF

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 8

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits <u>3/</u>		Unit
					Min	Max	
Digital specifications - continued.							
Low voltage differential signaling (LVDS) outputs section							
Differential output voltage	V _T	3 mA mode	+25°C	01	620 typical		mV _{pp}
Output offset voltage	V _{OS}	3 mA mode	-55°C to +125°C	01	950	980	mV
Output rise time	t _R		+25°C	01	500 typical		ps
Output fall time	t _F		+25°C	01	500 typical		ps
CMOS output section							
Voltage output high	V _{OH}	I _{OH} = -500 μA	-55°C to +125°C	01	O _{VDD} - 0.3		V
Voltage output low	V _{OL}	I _{OL} = 1 mA	-55°C to +125°C	01		0.3	V
Output rise time	t _R		+25°C	01	1.8 typical		ns
Output fall time	t _F		+25°C	01	1.3 typical		ns
Switching specifications		See figures 4 and 5					
ADC output section							
Aperture delay	t _A		+25°C	01	375 typical		ps
RMS aperture jitter	j _A		+25°C	01	60 typical		fs
Output clock to <u>9/ 10/</u> data propagation delay, LVDS mode	t _{DC}	DDR rising edge	-55°C to +125°C	01	-260	120	ps
		DDR falling edge			-160	230	
		SDR rising edge			-260	230	

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 9

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits <u>3/</u>		Unit
					Min	Max	
Switching specifications							
ADC output section - continued.		See figures 4 and 5.					
Output clock to <u>9/</u> data propagation delay, CMOS mode	t _{DC}	DDR rising edge	-55°C to +125°C	01	-220	200	ps
		DDR falling edge			-310	110	
		SDR rising edge			-310	200	
Latency (pipeline delay)	L		+25°C	01	7.5 typical		cycles
Overvoltage recovery	t _{OVr}		+25°C	01	1 typical		cycles
SPI interface section		<u>10/ 11/ 12/</u>	See figures 8 and 9.				
SCLK period	t _{CLK}	Write operation	-55°C to +125°C	01	16		cycles <u>8/</u>
		Read operation			66		cycles
SCLK duty cycle	t _{HI} / t _{CLK} or t _{LO} / t _{CLK}	Read or write	-55°C to +125°C	01	25	75	%
CSB↓ to SCLK↑ setup time	t _S	Read or write	-55°C to +125°C	01	1		cycles
CSB↑ after SCLK↑ hold time	t _H	Read or write	-55°C to +125°C	01	3		cycles
Data valid to SCK↑ setup time	t _{DSW}	Write	-55°C to +125°C	01	1		cycles
Data valid after SCK↑ hold time	t _{DHW}	Write	-55°C to +125°C	01	3		cycles

See footnotes at end of table.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 10

TABLE I. Electrical performance characteristics – Continued. 1/

Test	Symbol	Conditions <u>2/</u>	Temperature, T _A	Device type	Limits <u>3/</u>		Unit
					Min	Max	
Switching specifications							
SPI interface section - continued. <u>10/ 11/ 12/</u> See figures 8 and 9.							
Data valid after SCK↓ time	t _{DVR}	Read	-55°C to +125°C	01		16.5	cycles
Data invalid after SCK↑ time	t _{DHR}	Read	-55°C to +125°C	01	3		cycles
Sleep mode <u>13/</u> CSB↓ to SCLK↑ setup time	t _S	Read or write in sleep mode	-55°C to +125°C	01	150		μs

- 1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.
- 2/ Unless otherwise specified, AVDD = 1.8 V, OVDD = 1.8 V, A_{IN} = -1 dBFS, f_{SAMPLE} = maximum conversion rate (per speed grade).
- 3/ Parameters with min and/or max limits are 100% production tested at their worst case temperature extreme (+125°C).
- 4/ Digital supply current is dependent upon the capacitive loading of the loading of the digital outputs. I_{OVDD} specifications apply for 10 pF load on each digital output.
- 5/ See nap / sleep mode description in the datasheet for more details
- 6/ AC specifications apply after internal calibration of the analog digital converter is invoked at the given sample rate and temperature. Refer to “power on calibration” and “user initiated reset” in the device datasheet for more details.
- 7/ The DLL range setting must be changed for low speed operation.
- 8/ The tri-level inputs internal switching thresholds are approximately 0.43 V and 1.34 V. It is advised to float the inputs, tie to ground or AVDD depending on desired function.
- 9/ The input clock to output clock delay is a function of sample rate, using the output clock to latch the data simplifies data capture for most application.
- 10/ Parameter guaranteed by characterization and not 100% tested.
- 11/ Serial peripheral interface (SPI) interface timing is directly proportional to the ADC sample period (t_S). 4 ns at 250 MSPS. Minimum and maximum limits guaranteed by characterization, and not 100% tested.
- 12/ The SPI may operate asynchronously with respect to the ADC sample clock.
- 13/ The SPI chip select (CSB) setup time increases in sleep mode due to the reduced power state, CSB setup time in nap mode is equal to normal mode CSB setup time (4 ns minimum).

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 11

Case X

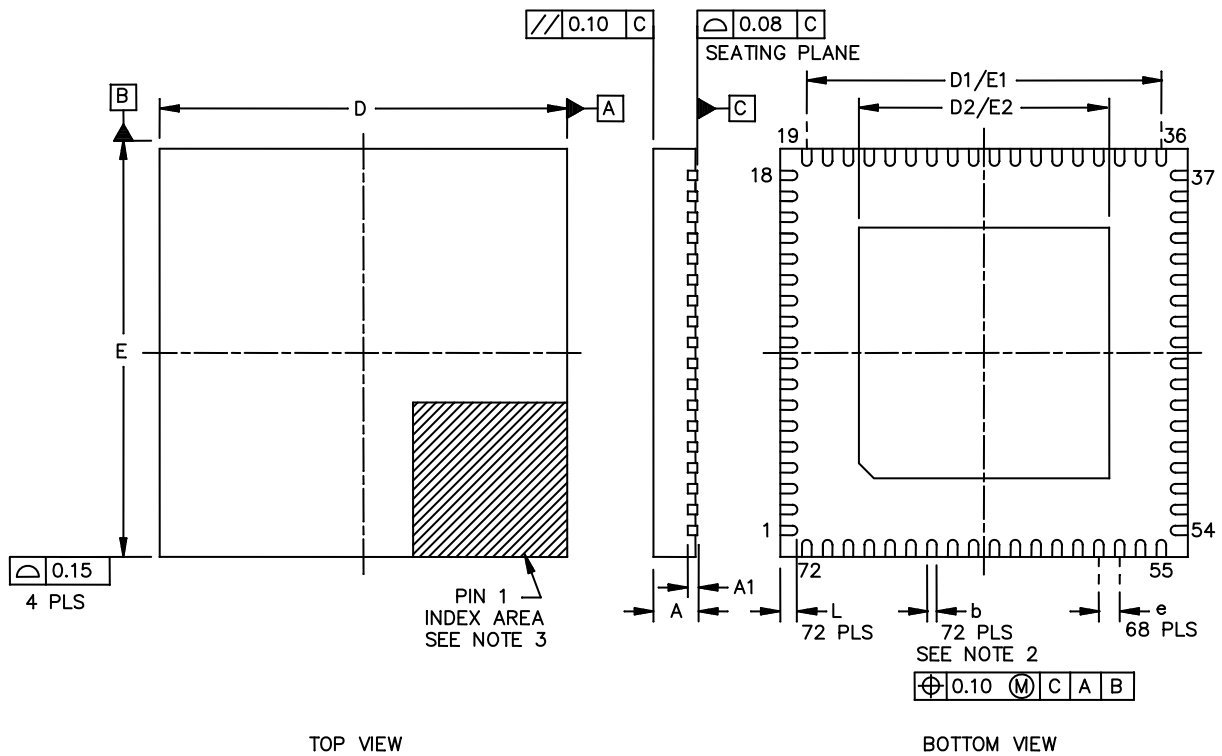


FIGURE 1. Case outline.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/10609</p>
		<p>REV</p>	<p>PAGE 12</p>

Case X - continued.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.035	---	0.90
A1	---	0.007	---	0.2
b	0.009	---	0.24	---
D/E	0.393 BSC		10.00 BSC	
D1/E1	0.334 BSC		8.50 BSC	
D2/E2	0.236 BSC		6.00 BSC	
e	0.019 BSC		0.50 BSC	
L	0.015	---	0.40	---
N	72		72	

NOTES:

1. Controlling dimensions are millimeter, inch dimensions are given for reference only.
2. Dimension b applies to the metalized terminal and is measured between 0.15 mm (inch) and 0.30 mm (inch) from the terminal tip.
3. The configuration of the pin 1 identifier is optional, but must be located within the zone indicated. The pin 1 identifier may be either a mold or mark feature.

FIGURE 1. Case outline - continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 13

Device type	01				
Case outline	X				
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AVDD	25	RESETN	49	D6N
2	DNC	26	OVSS	50	D6P
3	DNC	27	OVDD	51	D7N
4	DNC	28	DNC	52	D7P
5	DNC	29	DNC	53	D8N
6	AVDD	30	DNC	54	D8P
7	AVSS	31	DNC	55	OVSS
8	AVSS	32	D0N	56	OVDD
9	VINN	33	D0P	57	D9N
10	VINP	34	D1N	58	D9P
11	AVSS	35	D1P	59	D10N
12	AVDD	36	OVDD	60	D10P
13	DNC	37	D2N	61	D11N
14	DNC	38	D2P	62	D11P
15	VCM	39	D3N	63	ORN
16	CLKDIV	40	D3P	64	ORP
17	DNC	41	D4N	65	OVSS
18	DNC	42	D4P	66	SDO
19	AVDD	43	D5N	67	CSB
20	CLKP	44	D5P	68	SCLK
21	CLKN	45	OVSS	69	SDIO
22	OUTMODE	46	RLVDS	70	OUTFMT
23	NAPSLP	47	CLKOUTN	71	AVDD
24	AVDD	48	CLKOUTP	72	AVSS

FIGURE 2. Terminal connections.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 14

Terminal symbol	LVDS function SDR mode	DDR mode comments
AVDD	1.8 V analog supply.	
DNC	Do not connect.	
AVSS	Analog ground.	
VINN, VINP	Analog input negative, positive.	
VCM	Common mode output.	
CLKDIV	Clock divider control.	
CLKP, CLKN	Clock input true, complement.	
OUTMODE	Output mode (LVDS).	
NAPSLP	Power control, (nap, sleep modes).	
RESETN	Power on reset (active low).	
OVSS	Output ground.	
OVDD	1.8 V output supply.	
D0N	LVDS bit 0 (LSB) output complement.	DDR logical bits 1, 0 (LVDS)
D0P	LVDS bit 0 (LSB) output true.	DDR logical bits 1, 0 (LVDS)
D1N	LVDS bit 1 output complement.	NC in DDR
D1P	LVDS bit 1 output true.	NC in DDR
D2N	LVDS bit 2 output complement.	DDR logical bits 3, 2 (LVDS)
D2P	LVDS bit 2 output true.	DDR logical bits 3, 2 (LVDS)
D3N	LVDS bit 3 output complement.	NC in DDR
D3P	LVDS bit 3 output true.	NC in DDR
D4N	LVDS bit 4 output complement.	DDR logical bits 5, 4 (LVDS)
D4P	LVDS bit 4 output true.	DDR logical bits 5, 4 (LVDS)
D5N	LVDS bit 5 output complement.	NC in DDR
D5P	LVDS bit 5 output true.	NC in DDR

FIGURE 2. Terminal connections - continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 15

Terminal symbol	LVDS function SDR mode	DDR mode comments
RLVDS	LVDS bias resistor (connect to OVSS with a 10 k Ω 1% resistor).	
CLKOUTN	LVDS clock output complement.	
CLKOUTP	LVDS clock output true.	
D6N	LVDS bit 6 output complement.	DDR logical bits 7, 6 (LVDS)
D6P	LVDS bit 6 output true.	DDR logical bits 7, 6 (LVDS)
D7N	LVDS bit 7 output complement.	NC in DDR
D7P	LVDS bit 7 output true.	NC in DDR
D8N	LVDS bit 8 output complement.	DDR logical bits 9, 8 (LVDS)
D8P	LVDS bit 8 output true.	DDR logical bits 9, 8 (LVDS)
D9N	LVDS bit 9 output complement.	NC in DDR
D9P	LVDS bit 9 output true.	NC in DDR
D10N	LVDS bit 10 output complement.	DDR logical bits 11, 10 (LVDS)
D10P	LVDS bit 10 output true.	DDR logical bits 11, 10 (LVDS)
D11N	LVDS bit 11 output complement.	NC in DDR
D11P	LVDS bit 11 output true.	NC in DDR
ORN	LVDS over range complement.	
ORP	LVDS over range true.	
SDO	Serial peripheral interface (SPI) serial data output (4.7 k Ω pull-up to OVDD is required).	
CSB	SPI chip select (active low).	
SCLK	SPI clock.	
SDIO	SPI serial data input/output.	
OUTFMT	Output data format (two's complement, gray code, offset binary).	
AVSS	Analog ground.	

NOTE: SDR is the default state at power up the package.

FIGURE 2. Terminal connections - continued.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 16

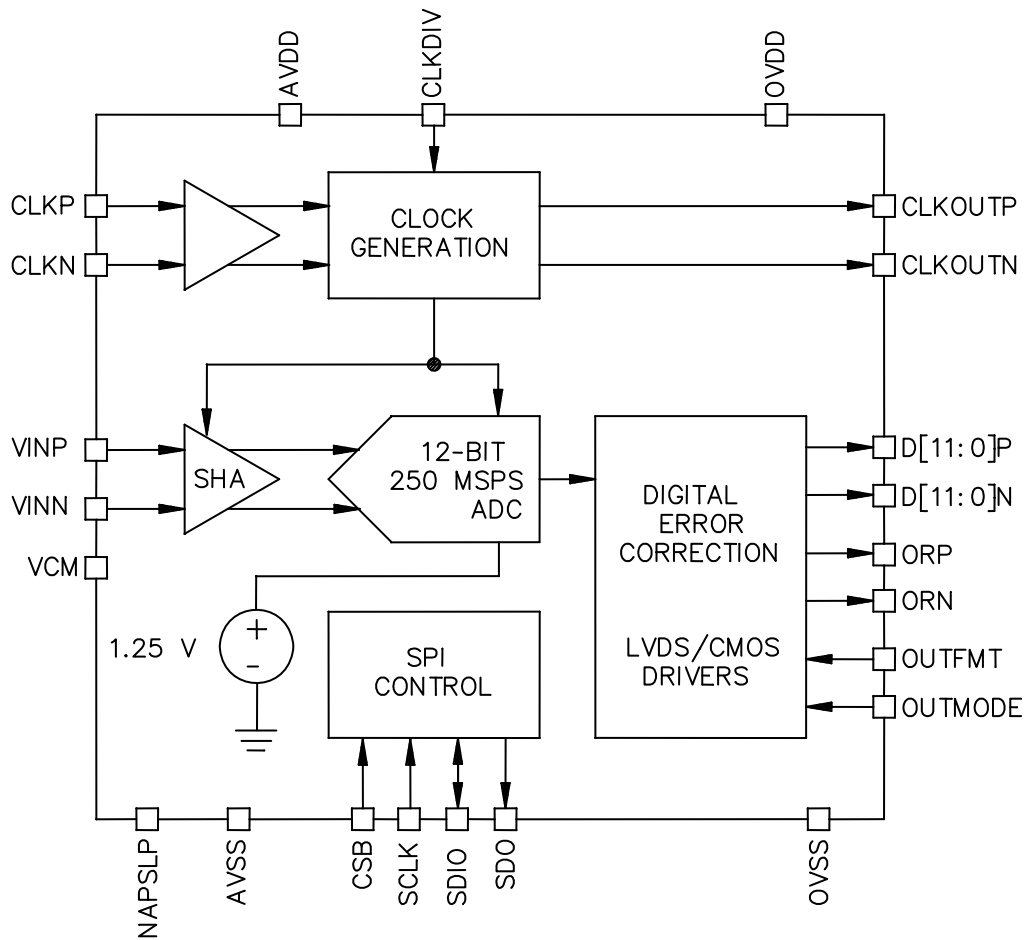


FIGURE 3. Block diagram.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 17

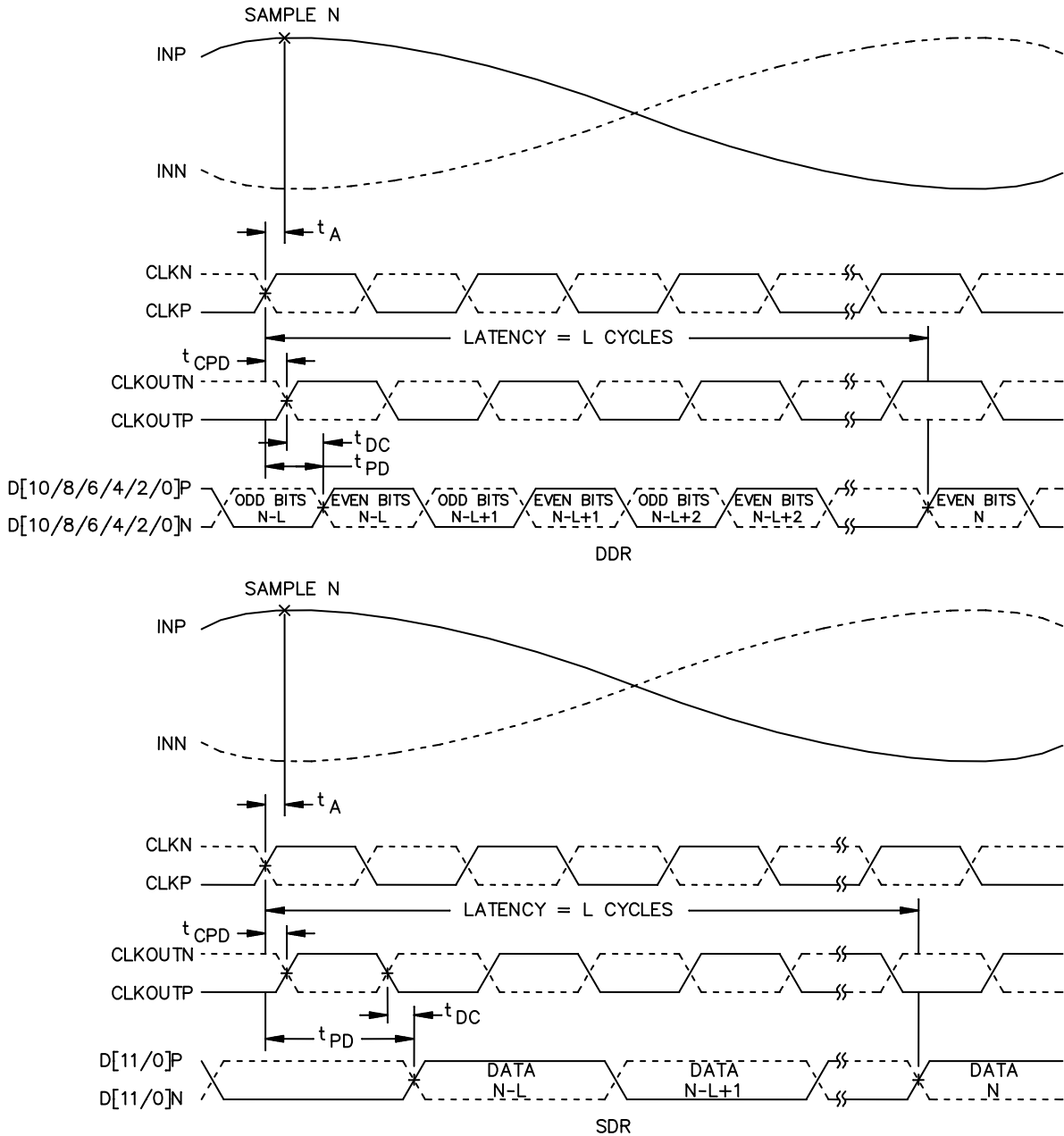


FIGURE 4. LVDS timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 18

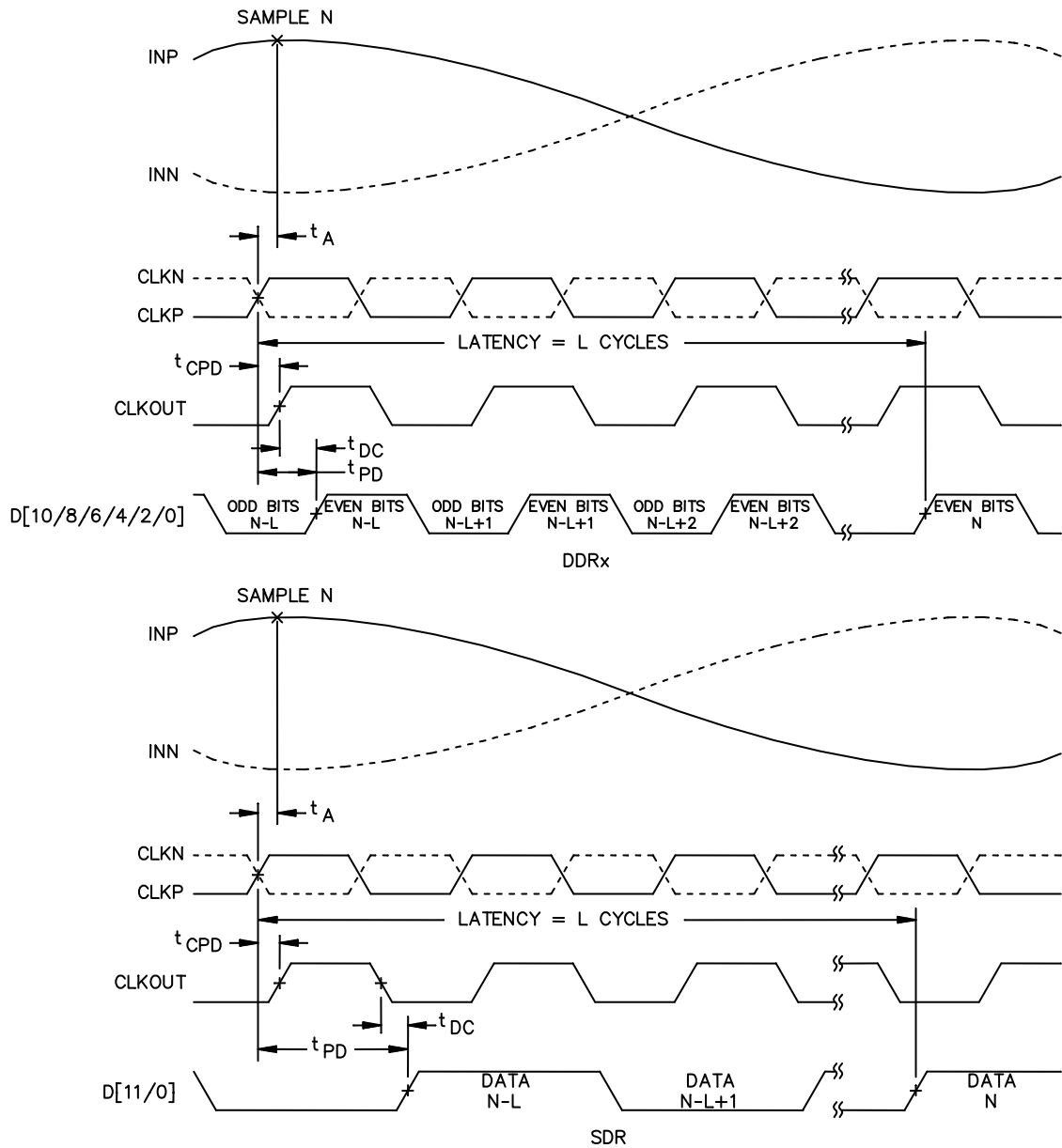


FIGURE 5. CMOS timing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 19

Input voltage	Offset binary	Two's complement	Gray code
-Full scale	000 00 000 00 00	100 00 000 00 00	000 00 000 00 00
-Full scale + 1 LSB	000 00 000 00 01	100 00 000 00 01	000 00 000 00 01
Mid-scale	100 00 000 00 00	000 00 000 00 00	110 00 000 00 00
+Full scale - 1 LSB	111 11 111 11 10	011 11 111 11 10	100 00 00 00 01
+Full scale	111 11 111 11 11	011 11 111 111 1	100 00 000 00 00

Input voltage to output code mapping

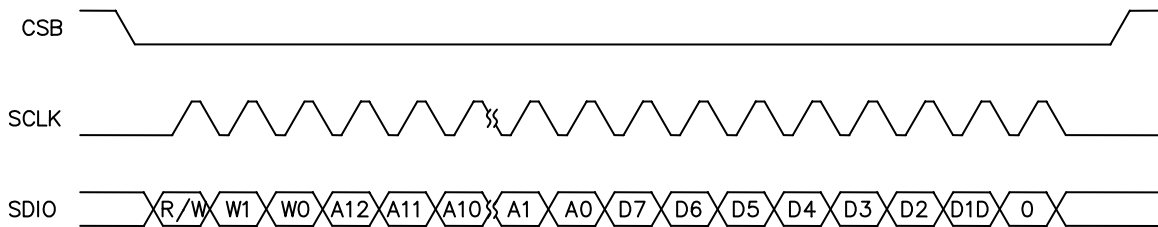


FIGURE 6. MSB first addressing waveforms.

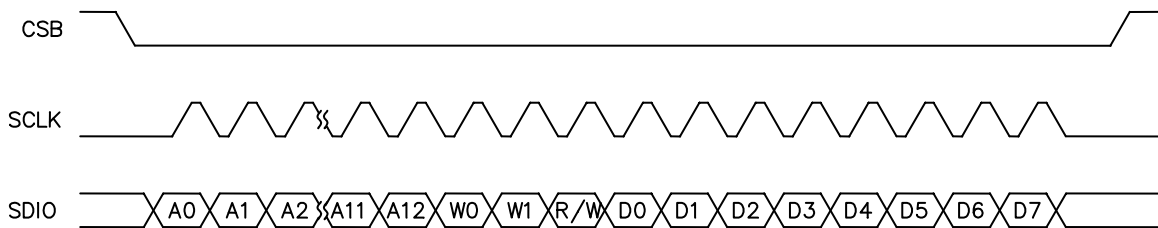


FIGURE 7. LSB first addressing waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 20

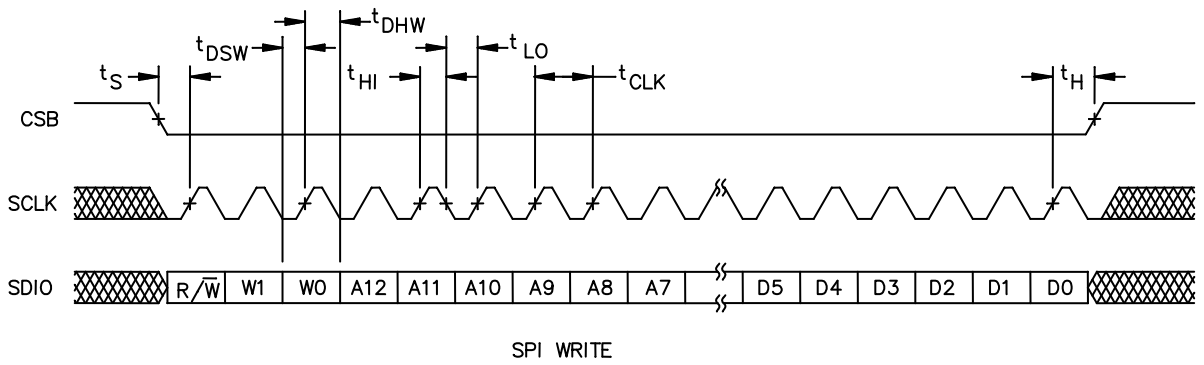


FIGURE 8. SPI write waveforms.

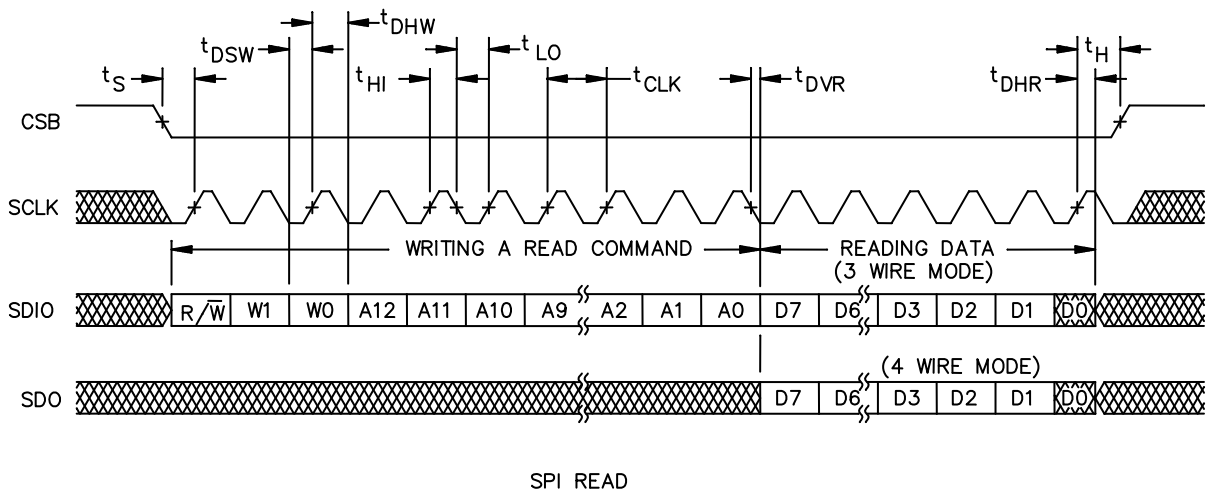


FIGURE 9. SPI read waveforms.

<p>DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO</p>	<p>SIZE A</p>	<p>CODE IDENT NO. 16236</p>	<p>DWG NO. V62/10609</p>
		<p>REV</p>	<p>PAGE 21</p>

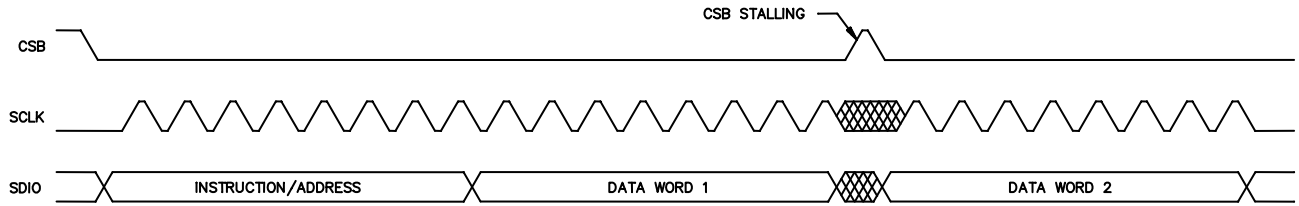


FIGURE 10. 2 byte transfer waveforms.

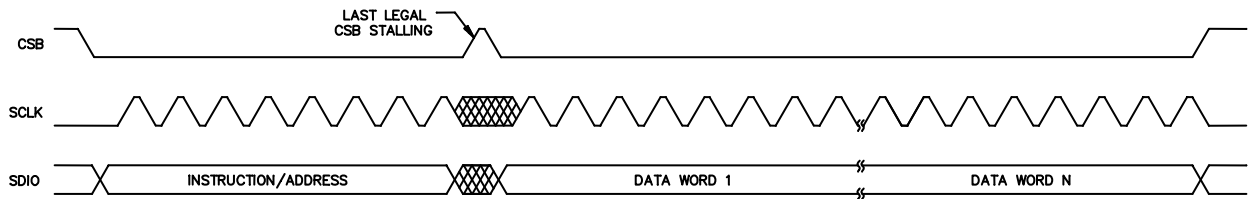


FIGURE 11. N byte transfer waveforms.

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 22

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item.

Vendor item drawing administrative control number <u>1/</u>	Device manufacturer CAGE code	Part marking <u>2/</u>	Vendor part number
V62/10609-01XE	34371	ISLA112P25MREP	ISLA112P25MREP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

2/ This lead (Pb) free plastic package employ special Pb free material sets; molding compounds/die attach materials and nickel (Ni), Pb, and gold (Au) plate - precious metals (e4) termination finish, which Restriction of Hazardous Substances Directive (RoHS) compliant and compatible with both tin lead (SnPb) and Pb free soldering operations. This Pb free device is moisture sensitivity level (MSL) classified at Pb free peak reflow temperatures that meet or exceed the Pb free requirements of IPC/JEDEC J STD-020.

CAGE code

34371

Source of supply

Intersil Corporation
 1001 Murphy Ranch Road
 Milpitas, CA 95035-6803
 Point of contact: 1650 Robert J. Conlan Blvd.
 Palm Bay, FL 32905

DEFENSE SUPPLY CENTER, COLUMBUS COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/10609
		REV	PAGE 23