

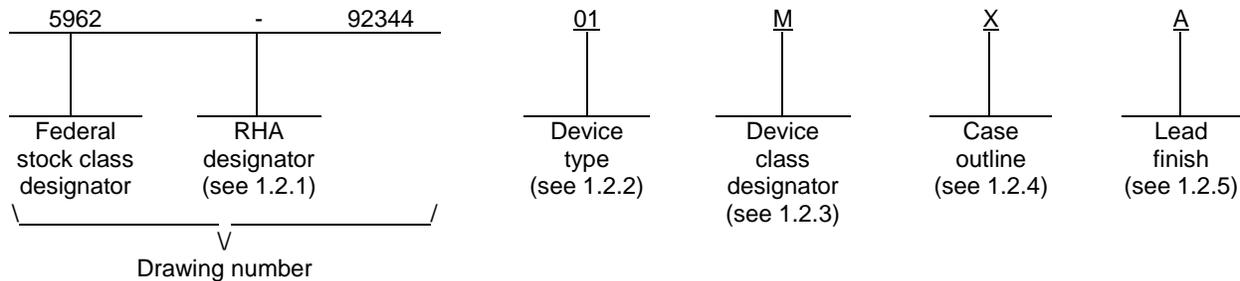
REVISIONS																			
LTR	DESCRIPTION																DATE (YR-MO-DA)		APPROVED
A	Updated boilerplate to current requirements. lhl																13-02-06		Charles F. Saffle

REV																					
SHEET																					
REV	A	A	A	A	A	A	A														
SHEET	15	16	17	18	19	20	21														
REV STATUS OF SHEETS				REV				A	A	A	A	A	A	A	A	A	A	A	A		
				SHEET				1	2	3	4	5	6	7	8	9	10	11	12	13	14
PMIC N/A				PREPARED BY Jeff Bowling				DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil													
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Jeff Bowling																	
				APPROVED BY Michael A. Frye																	
				DRAWING APPROVAL DATE 93-12-16																	
				REVISION LEVEL A																	
				SIZE A		CAGE CODE 67268		5962-92344													
				SHEET 1 OF 21																	

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device class V), high reliability (device class M and Q). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device class Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>	<u>Access time</u>
01	71B74	8K X 8 SRAM, resettable	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}).....	-0.5 V dc to +7.0 V
Voltage on any pin with respect to GND (V_{TERM}) range.....	-0.5 V dc to +7.0 V 2/ 3/
Storage temperature range.....	-65°C to +150°C
Thermal resistance, junction-to-case (θ_{JC}).....	20°C/W
Junction temperature.....	150°C
Power dissipation.....	1.0 W
DC output current.....	50 mA
Terminal soldering, temperature range (10 seconds).....	275°C

1.4 Recommended operating conditions.

Supply voltage range.....	4.5 V dc to 5.5 V dc
High level input voltage range (V_{IH}).....	2.2 V dc to 6.0 V dc 2/ 3/
Low level input voltage range (V_{IL}).....	-0.5 V dc to +0.8 V dc 4/
Case operating temperature range (T_C).....	55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
 MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
 MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DoDISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DoDISS are the issues of the documents cited in the solicitation.

JEDEC – JEDEC INTERNATIONAL

JESD 78 - IC Latch-Up Test.

(Copies of this document are available online at www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201)

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ V_{TERM} must not exceed $V_{CC} + 0.5$ V.
- 3/ All inputs except reset.
- 4/ V_{IL} (min) = -3.0 V for pulse width less than 5 ns.

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2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table(s) shall be as specified on figure 2.

3.2.4 Functional algorithms. Various functional algorithms used to test this device are contained in appendix A (herein). If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device classes Q and V, alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.2.5 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

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3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 042 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input leakage current	I _{LI}	V _{CC} = maximum V _{IN} = GND to V _{CC}	1, 2, 3		10.0	μA
Output leakage current	I _{LO}	V _{CC} = maximum V _{OUT} = GND to V _{CC} CS = V _{IH}	1, 2, 3		10.0	μA
Input LOW level voltage	V _{IL}		1, 2, 3	-0.5	0.8	V
Input HIGH level voltage (except for RESET input)	V _{IH}	All inputs except $\overline{\text{RESET}}$ input	1, 2, 3	2.2	V _{CC} +0.5	V
Input HIGH level voltage (for RESET input)	V _{IHR}	For $\overline{\text{RESET}}$ input only	1, 2, 3	2.5	V _{CC} +0.5	V
Output LOW voltage (MATCH output)	V _{OL1}	MATCH output I _{OL} = 18 mA V _{CC} = minimum	1, 2, 3		0.4	V
Output LOW voltage (MATCH output)	V _{OL2}	MATCH output I _{OL} = 22 mA V _{CC} = minimum	1, 2, 3		0.5	V
Output HIGH voltage (except MATCH output)	V _{OL3}	I _{OL} = 10 mA V _{CC} = minimum Except MATCH output	1, 2, 3		0.5	V
Output LOW voltage (except MATCH output)	V _{OL4}	I _{OL} = 8 mA V _{CC} = minimum Except MATCH output	1, 2, 3		0.4	V
Output HIGH voltage (except MATCH output)	V _{OH}	I _{OH} = -4 mA V _{CC} = minimum	1, 2, 3	2.4		V
Dynamic operating current	I _{CC1}	V _{CC} = maximum f = f _{MAX} 1/, $\overline{\text{CS}} = V_{IL}$, $\overline{\text{WE}} = V_{IL}$ I _{OUT} = 0 mA, $\overline{\text{CS}} = V_{IL}$, $\overline{\text{WE}} = V_{IL}$	1, 2, 3		190	mA
Dynamic operating current	I _{CC2}	V _{CC} = maximum f = f _{MAX} 1/, $\overline{\text{CS}} = V_{IL}$, $\overline{\text{WE}} = V_{IL}$ I _{OUT} = 0 mA, $\overline{\text{CS}} = V_{IL}$, $\overline{\text{WE}} = V_{IL}$	1, 2, 3		160	mA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Input capacitance	C _{IN}	V _{IN} = 0V, f = 1 MHz, See 4.4.1e <u>2/</u>	4		7	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V, f = 1 MHz, See 4.4.1e <u>2/</u>	4		8	pF
Functional tests		See 4.4.1c	7, 8A, 8B			
READ CYCLE TIMING						
Read cycle time	t _{AVAV}	<u>3/</u>	9, 10, 11	20		ns
Address access time	t _{AVQV}		9, 10, 11		20	ns
Chip Select access time	t _{SLQV}		9, 10, 11		10	ns
Chip Select to output in LOW Z <u>2/</u>	t _{SLQX}		9, 10, 11	3		ns
Output enable to output valid	t _{OLQV}		9, 10, 11		9	ns
Output enable to output in LOW Z <u>2/</u>	t _{OLQX}		9, 10, 11	2		ns
Chip Select to output in HIGH Z <u>2/</u>	t _{SHQZ}		9, 10, 11		8	ns
Output disable to output in HIGH Z <u>2/</u>	t _{OHQZ}		9, 10, 11		8	ns
Output hold from address change	t _{AVQX}		9, 10, 11	3		ns
WRITE CYCLE TIMING						
WRITE cycle time	t _{AVAV}	<u>3/</u>	9, 10, 11	20		ns
Chip Select to end of write	t _{SLSH}		9, 10, 11	15		ns
Address valid to end of write	t _{AVSH}		9, 10, 11	15		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
WRITE CYCLE TIMING						
Address setup time	t _{AVWL}	<u>3/</u>	9, 10, 11	0		ns
Write pulse width	t _{WLWH}		9, 10, 11	15		ns
Write recovery time	t _{WHAV}		9, 10, 11	0		ns
Write enable to output in HIGH Z <u>2/</u>	t _{WLQZ}		9, 10, 11		5	ns
Data valid to end of Write	t _{DVWH}		9, 10, 11	10		ns
Data Hold from Write time	t _{WHDX}		9, 10, 11	0		ns
Output active from end of Write <u>2/</u>	t _{WHQV}		9, 10, 11	2		ns
MATCH CYCLE TIMING						
Address to MATCH valid	t _{ADM}	<u>3/</u>	9, 10, 11		20	ns
Chip Select to MATCH valid	t _{CSM}		9, 10, 11		10	ns
Chip select to MATCH HIGH	t _{CSMHI}	<u>2/ 3/</u>	9, 10, 11		8	ns
Data input to MATCH valid	t _{DAM}	<u>3/</u>	9, 10, 11		12	ns
\overline{OE} LOW to MATCH HIGH	t _{OEMHI}	<u>2/ 3/</u>	9, 10, 11		10	ns
\overline{WE} LOW MATCH HIGH	t _{WEMHI}		9, 10, 11		10	ns
\overline{RESET} LOW to MATCH HIGH	t _{RSMHI}		9, 10, 11		15	ns
MATCH valid Hold from address	t _{MHA}	<u>3/</u>	9, 10, 11	2		ns
MATCH valid Hold from Data	t _{MHD}	<u>3/</u>	9, 10, 11	2		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
RESET TIMING						
$\overline{\text{RESET}}$ pulse width	t _{RSPW}	<u>3/</u> <u>4/</u>	9, 10, 11	60		ns
$\overline{\text{WE}}$ HIGH to $\overline{\text{RESET}}$ HIGH	t _{WERS}	<u>3/</u>	9, 10, 11	5		ns
$\overline{\text{RESET}}$ HIGH to $\overline{\text{WE}}$ LOW	t _{RSRC}	<u>3/</u>	9, 10, 11	30		ns
Power ON RESET	t _{PORS}	<u>2/</u> <u>3/</u>	9, 10, 11	120		ns

- 1/ At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{AVAV}.
- 2/ This parameter tested initially and after any design or process change which could affect this parameter, and therefore shall be guaranteed to the limits specified in table I.
- 3/ See figure 3 for output load circuits and test conditions, and see figure 4 for timing waveforms.
- 4/ Recommend duty cycle = 10% maximum.

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Pin	Function
1	NC
2	$\overline{\text{RESET}}$
3	A ₁₂
4	A ₇
5	A ₆
6	A ₅
7	A ₄
8	A ₃
9	A ₂
10	A ₁
11	A ₀
12	NC
13	I/O ₀
14	I/O ₁
15	I/O ₂
16	GND
17	NC
18	I/O ₃
19	I/O ₄
20	I/O ₅
21	I/O ₆
22	I/O ₇
23	$\overline{\text{CS}}$
24	A ₁₀
25	$\overline{\text{OE}}$
26	NC
27	A ₁₁
28	A ₉
29	A ₈
30	MATCH
31	$\overline{\text{WE}}$
32	V _{CC}

FIGURE 1. Terminal connections.

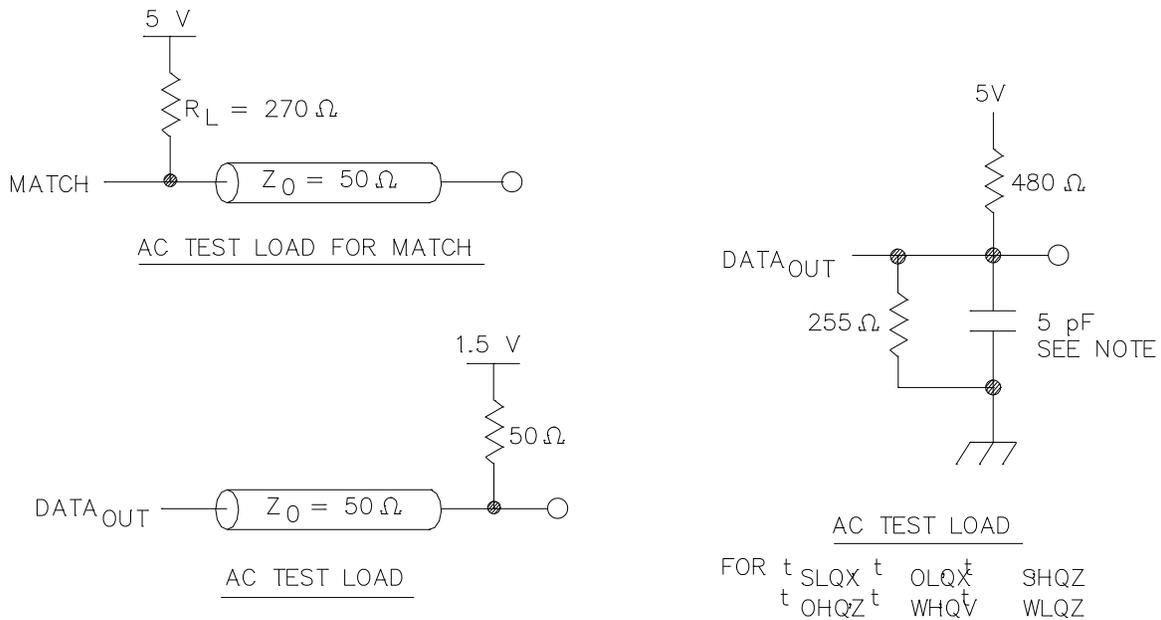
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\overline{WE}	\overline{CS}	\overline{OE}	\overline{RESET}	MATCH	I/O	Function
X	X	X	L	H	X	Reset all bits to LOW
X	H	X	H	H	HI Z	Deselect chip
H	L	H	H	L	D _{IN}	No match
H	L	H	H	H	D _{IN}	MATCH
H	L	L	H	H	D _{OUT}	Read
L	L	X	H	H	D _{IN}	Write

NOTES:

1. X can be V_{IL} or V_{IH} .
2. H = V_{IH} , L = V_{IL} .

FIGURE 2. Truth table.



AC TEST CONDITIONS

INPUT PULSE LEVELS	GND TO 3.0 V
INPUT RISE/FALL TIMES	≤ 3 ns
INPUT TIMING REFERENCE LEVELS	1.5 V
OUTPUT REFERENCE LEVEL	1.5 V

NOTE: Capacitance includes scope and jig.

FIGURE 3. Load circuits.

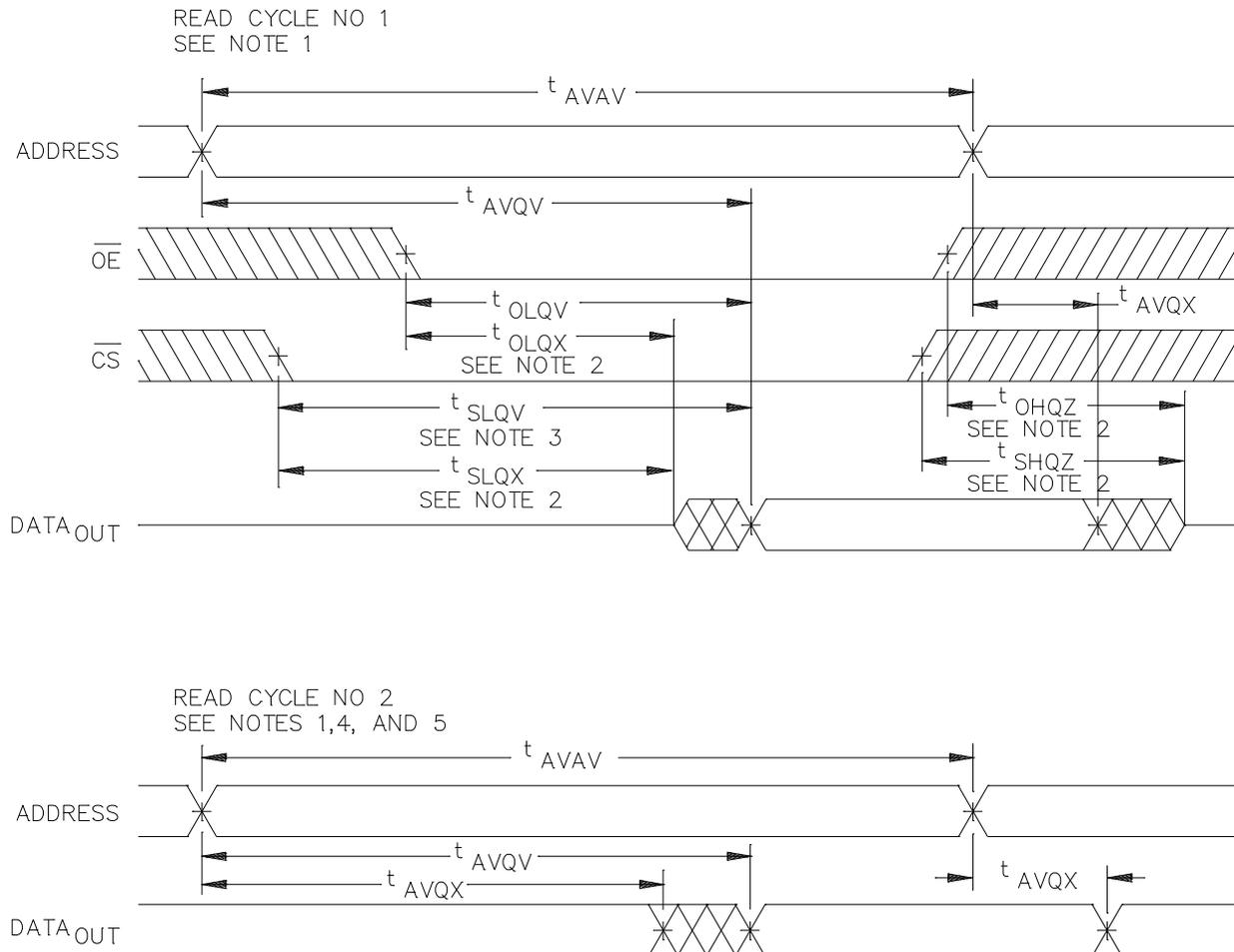
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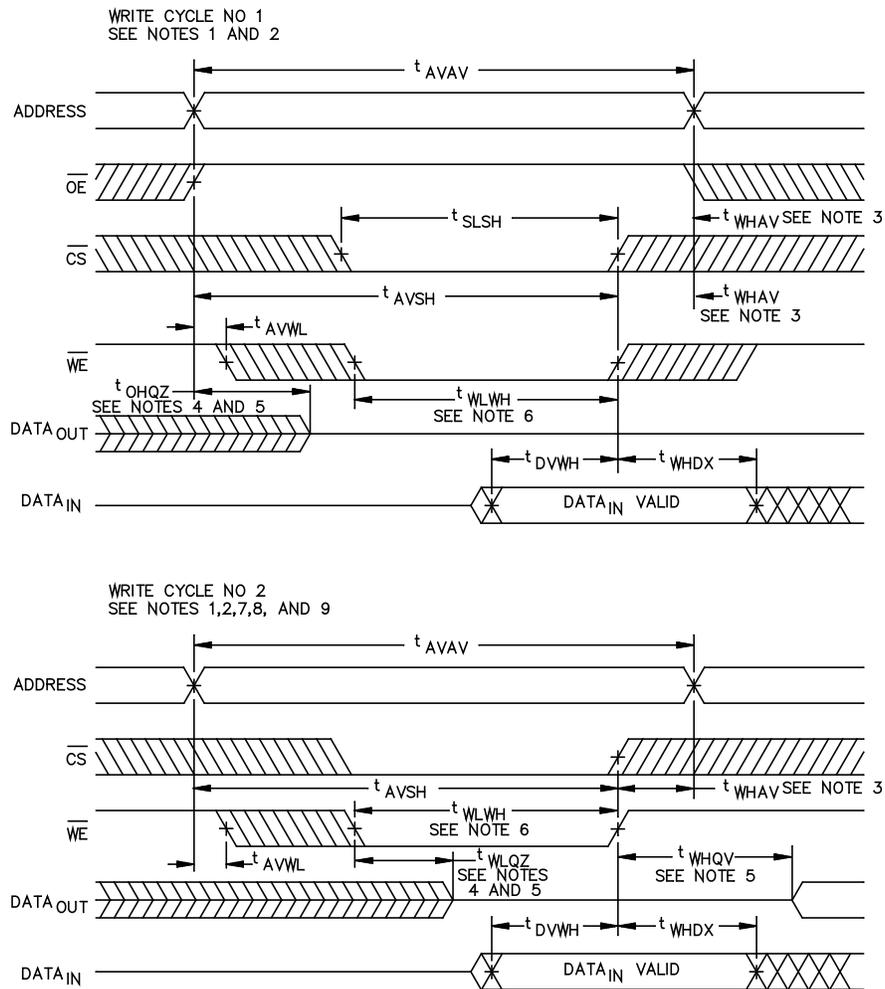


NOTES:

1. WE is high for read cycle.
2. Transition is measured ± 200 mV from steady state.
3. Address valid prior to or coincident with CS transition low.
4. Device is continuously selected, CS = V_{IL}.
5. OE = V_{IL}.

FIGURE 4. Timing waveforms.

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NOTES:

1. \overline{WE} , \overline{CS} must be inactive during all address transitions.
2. If the \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, the outputs remain in a high impedance state.
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. Transition is measured $\pm 200\text{mV}$ from steady state.
6. A write occurs during the overlap (t_{WP}) of a low \overline{WE} and a low \overline{CS} .
7. \overline{OE} is continuously low ($\overline{OE} = V_{IL}$).
8. $DATA_{OUT}$ is the same phase of write data of this write cycle.
9. If \overline{CS} is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.

FIGURE 4. Timing waveforms – Continued.

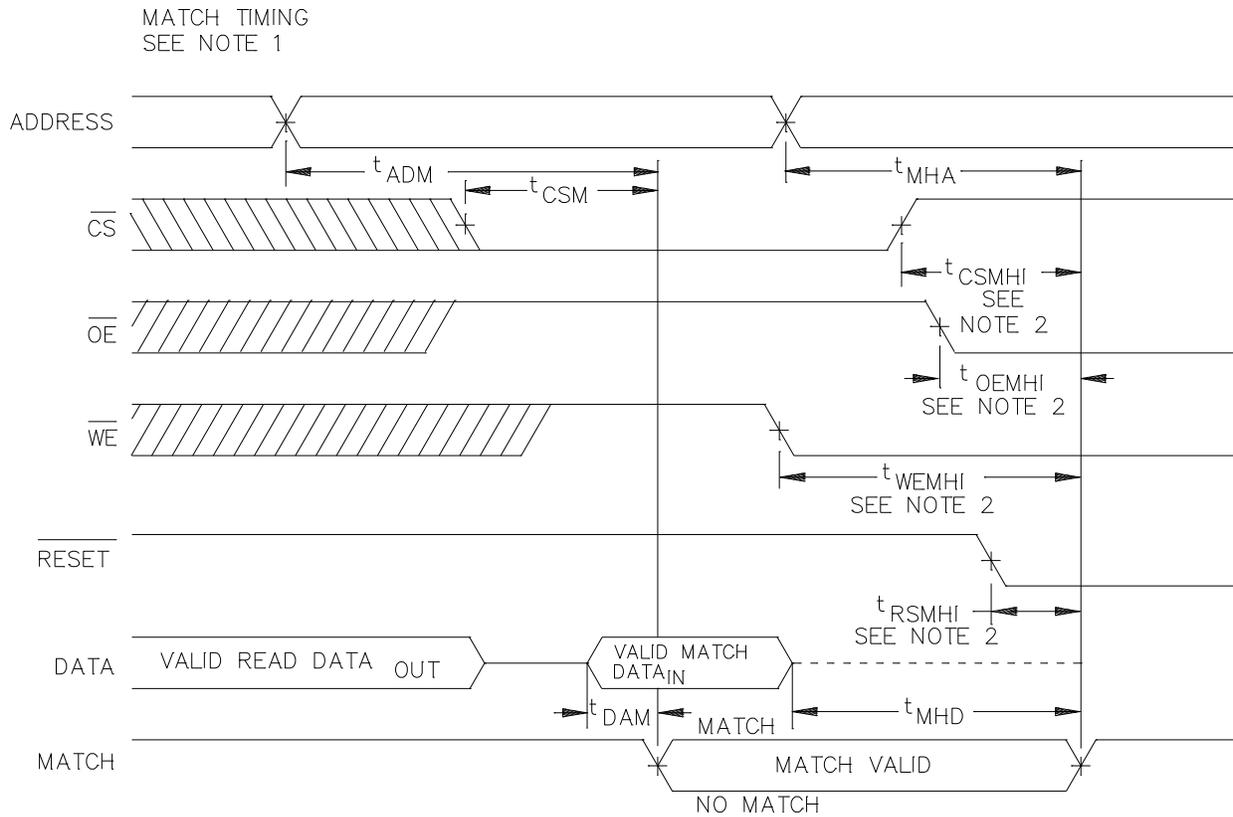
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- NOTES:
1. It is not recommended to float data and address inputs while the MATCH pin is active.
 2. Transition is measured at $\pm 200\text{mV}$ from steady state.

FIGURE 4. Timing waveforms – Continued.

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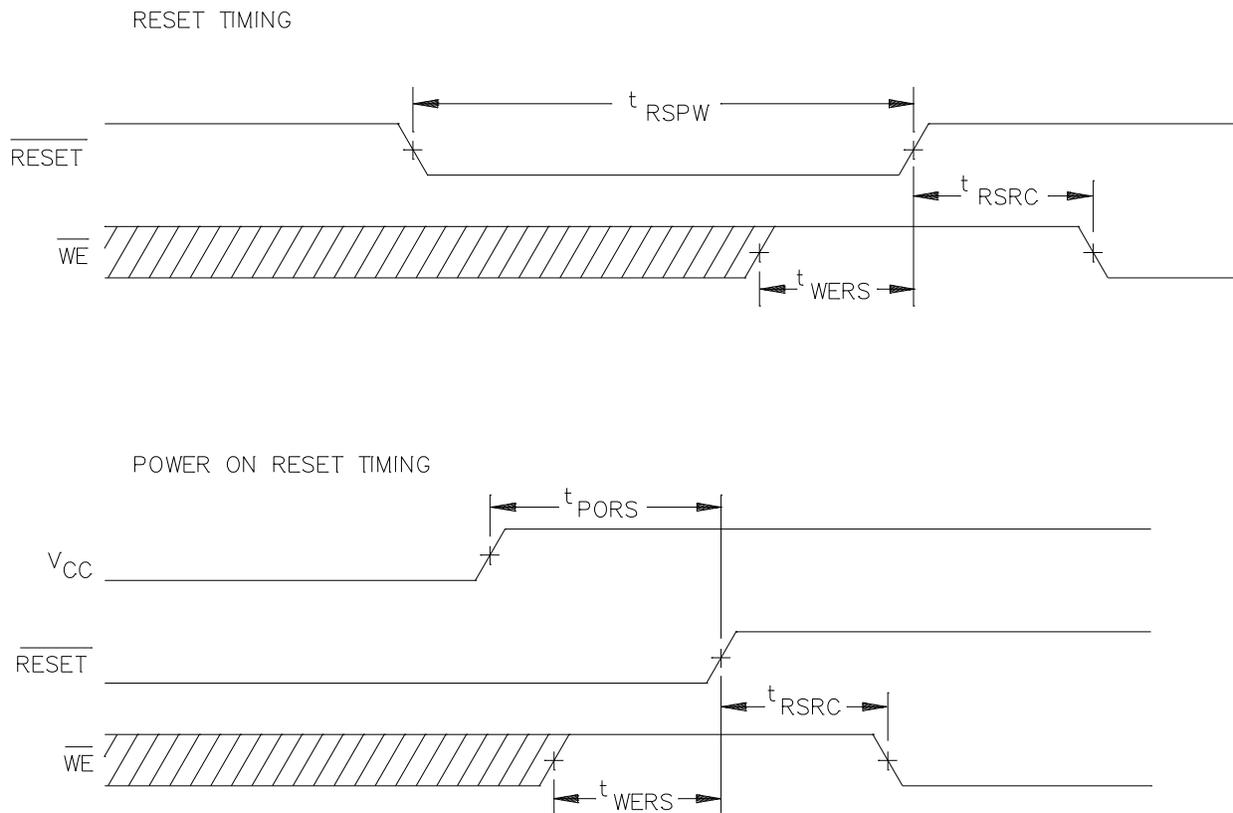


FIGURE 4. Timing waveforms – Continued.

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4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. Prior to burn-in, the devices shall be programmed <see 4.6.4 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot (see 4.2.3 herein).
- c. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
 - (2) $T_A = +125^{\circ}\text{C}$, minimum.
- d. Interim and final electrical test parameters shall be as specified in table IIA herein.
- e. After completion of all screening, the device shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B and as detailed in table IIB herein.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. 0/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class H, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with HIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JESD 78 may be used for reference.
- e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C and shall consist of test specified in table IIB herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}C$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}C \pm 5^{\circ}C$, after exposure, to the subgroups specified in table IIA herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
Static burn-in I and II method 1015	Not required	Not required	Required
Interim electrical parameters (see 4.2)			1*, 7* Δ
Dynamic burn-in (method 1015)	Required	Required	Required
Interim electrical parameters (see 4.2)			1*, 7* Δ
Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate test is not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * Indicates PDA applies to subgroups 1 and 7.

5/ ** See 4.4.1e.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters (see line 1, Interim Electrical Parameters).

7/ See 4.4.1d.

TABLE IIB. Delta limits at 25°C.

Parameter 1/	Device types
	All
I _{LI} , I _{LO}	± 10

1/ The above parameter shall be recorded before and after the required burn-in and life test to determine delta.

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4.5 Delta measurements for device classes Q and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7 and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

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APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-92344
FUNCTIONAL ALGORITHMS

A.1 SCOPE

A.1.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS This section is not applicable to this appendix.

A.3 ALGORITHMS

A.3.1 Algorithm A (pattern 1).

A.3.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from Location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from Location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from Location 0 to maximum.

A.3.2 Algorithm 8 (pattern 2).

A.3.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "O's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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APPENDIX A
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 FUNCTIONAL ALGORITHMS

A.3.3 Algorithm C (pattern 3).

A.3.3.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "O's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

A.3.4 Algorithm D (pattern 4).

A.3.4.1 CEDES- CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from Location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 13-02-06

Approved sources of supply for SMD 5962-92344 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <http://www.landandmaritime.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9234401MXA	<u>3/</u>	IDT71B74S20L32B

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ The last known source is listed below.

Vendor CAGE
number

61772

Vendor name
and address

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.